Atty. Docket No. PIA31224/DBE/US
Serial No: 10/751,198

Remarks

Applicant and their undersigned representative thank Examiner Wilson for the courteous and very helpful discussion held on February 7, 2006, regarding the present application. The claims have been amended as discussed to overcome the rejection in view of Moon et al. (U.S. Pat. Appl. Publ. No. 2002/0164838; hereinafter, "Moon et al."), and a Request for Continued Examination is filed herewith as suggested by the Examiner. The following remarks shall further summarize and expand upon other topics discussed.

The present invention relates to a method for packaging a multi-chip module, comprising:

a) connecting wafer bumps in a peripheral region of a first chip to lower parts of inner leads of first and second TAB tapes, each of the first and second TAB tapes having an inner lead and an outer lead;

b) connecting wafer bumps in a peripheral region of a second chip to upper parts of the inner leads of the first and second TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween;

c) mounting the outer lead of the first TAB tape on a patterned circuit;

d) connecting a third chip having thereon wafer bumps to an upper part of the second chip;

e) connecting an outer lead of the second TAB tape to at least one of the wafer bumps in a peripheral region of the third chip;

f) connecting an inner lead of a third TAB tape having the inner lead and an outer lead to at least one other wafer bump in the peripheral region of the third chip;

g) connecting wafer bumps in a peripheral region of a fourth chip to the outer lead of the second TAB tape and the inner lead of the third TAB tape; and

h) executing at least one encapsulation step, wherein an underfill material is filled in connecting portions between the first, second and third TAB tapes and the first, second, third and fourth chips (see amended claim 1 above).

The presently claimed invention is patentable over Moon et al., alone or together with Isaacson (U.S. Pat. No. 3,766,439; hereinafter, "Isaacson")) or Morrison et al. (U.S. Pat. Appl. Publ. No. 2002/0114143; hereinafter, "Morrison et al."), because of the connections made between the various TAB tapes and wafer bumps in the peripheral region of the various chips. As a result, the present application is believed to be in condition for allowance.

The Rejection of Claims 1, 2 and 11 under 35 U.S.C. § 102(e)

The rejection of Claims 1, 2 and 11 under 35 U.S.C. § 102(e) as being anticipated by Moon et al. is respectfully traversed.

Moon et al. discloses a method for increasing the integrated circuit density in a semiconductor assembly. The semiconductor assembly has an interposer substrate (which corresponds to the TAB tape of the present invention). The interposer substrate is attached to an active surface and a back side of a die and wraps around at least one side of the first die (Abstract of Moon et al., ll. 2-5; see also Figs. 1(c)-(d) of Moon et al.). The assembly may include a second die facing the first die and attached to the interposer substrate, the interposer substrate being wrapped around either the first or second die or, alternatively, being wrapped around both the first and second die (Abstract of Moon et al., last 5 lines).

A second embodiment of Moon et al. includes a first and second dice 110a and 110b (see also Fig. 3(a)). The first and second dice 110a and 110b each include an active surface 112 and a back side 114, and each may include conductive bumps such as solder bumps or gold stub bumps 116b formed on or attached to bond pads 116p on the active surfaces 112 thereof. The bond pads 116p may be formed in an arrangement such as one or more rows centrally located on the active surfaces 112 or, alternatively, arranged along a periphery thereof (paragraph [0039], p. 5 of Moon et al.).

The first and second dice 110 may be attached to first portion 236 of interposer substrate 230, either simultaneously or sequentially. Conductive traces 144 of interposer substrate 230 extend from metallization pads 242 to an array of conductive through vias 235 extending from a

first surface 232 of interposer substrate 230 to a second, opposing surface 234 (see paragraph [0040], p. 5, and Fig. 3(b) of Moon et al.).

This arrangement provides for the second portion 238 of the interposer (carrier) substrate 230, being freely extended laterally from first portion 238 and separated therefrom by spacer portion 240 as shown in FIG. 3(b), to fold or wrap around either a side 154 of the first die 110a (FIG. 3(c)) or a side 154 of the second die 110b (FIG. 3(d)). A non-conductive adhesive material 252 may be applied at any time prior to folding the carrier substrate 230 to be attached thereon, which may include applying the adhesive on the back sides 114 at the wafer level or subsequent to dicing the wafer. Thus, the second portion 238 of the carrier substrate 230 may fold around and be adhesively attached to either the back side 114 of the first die 110a or the back side 114 of the second die 110b, to form a stacked die assembly 260 (see paragraph [0041], p. 5, and Figs. 3(b)-(d) of Moon et al.).

By contrast, the present claim 1 recites connecting wafer bumps in peripheral regions of first and second chips to inner leads of ***first and second TAB tapes***, each of the first and second TAB tapes having an inner lead and an outer lead. Accordingly, Moon et al. do not disclose the method of claim 1, and the present claim 1 is not anticipated by Moon et al.

Claim 2 has been cancelled, and claim 11 depends from claim 1. Therefore, claim 11 include the same limitations as claim 1 above. As explained above, the interposer substrate in Moon et al. is connected to another assembly or a substrate using an array of conductive elements 172. Thus, for essentially the same reasons as for claim 1, claim 11 is not anticipated by Moon et al.

As a result, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 4 and 8 under 35 U.S.C. § 103

The rejection of Claims 4 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Moon et al. in view of Isaacson is respectfully traversed.

With regard to claim 1 above, Moon et al. further disclose a process for stacking third and fourth die on the first and second die. This variant of Moon et al. is similar to the second embodiment discussed above, except that the interposer substrate 330 is extended in length and comprises a first portion 336, first spacer portion 340a and two second portions 338a and 338b separated by a second spacer portion 340b (see paragraph [0045], pp. 5-6, and Figs. 4(a)-(b) of Moon et al.). With this configuration, the second portions 338a and 338b may be wrapped about the back sides 114 of both the first die 110a and the second die 110b by folding the two second portions 338a and 338b about the side 154 of one of the dice 110, covering that side 154 with the first spacer portion 340a, securing second portion 338a on the back side 114 of the one of the dice 110, then covering the two adjacent sides 154 of the dice 110 on the other side of the assembly with second spacer portion 340b and securing second portion 338b to the back side 114 of the other die 110 to form a stacked die assembly 360. Both second portions 338a and 338b may include an array of ball pads 135 to which traces 144 (not shown) extend from contact points with the bond pads of the dice 110. This variant thus provides both an upper outside surface 362 and a lower outside surface 364, on which discrete conductive elements 172 may be placed in an array corresponding to the pattern of ball pads 135. As in the second embodiment, the stacked die assembly 360 with discrete conductive elements 172 forming a chip scale package 370 may then be attached to terminal pads or other contacts of a carrier substrate such as a printed circuit board 182 or any other higher level packaging. However, in this variant, the chip scale package 370 may be stacked with one or more other chip scale packages 370 bearing discrete conductive elements 172, ***since the interposer substrate 330 wraps around both the upper and bottom outside surface 362 and 364***, to enable electrical connection with another stacked die assembly 360 (see paragraph [0045], pp. 5-6, and Figs. 4(a)-(b) of Moon et al.; emphasis added).

By contrast, the present claim 1 recites connecting wafer bumps in peripheral regions of first and second chips to inner leads of first and second TAB tapes, mounting the outer lead of the first TAB tape on a patterned circuit, connecting an outer lead of the second TAB tape to a wafer bump in a peripheral region of a third chip, connecting an inner lead of a third TAB tape to another wafer bump in the peripheral region of the third chip, and connecting wafer bumps in a

peripheral region of a fourth chip to the outer lead of the second TAB tape and the inner lead of the third TAB tape. Moon et al. do not disclose or suggest these steps in the method of claim 1, and therefore, Moon et al. is saliently deficient with regard to the present claim 1.

Isaacson fails to cure these deficiencies of Moon et al. Isaacson discloses an electronic circuit having utility in a multi-layer circuit board, formed of a flexible dielectric sheet of material to which is attached circuit runs etched from copper sheets clad to the dielectric sheet prior to etching (Abstract). Isaacson fails to disclose or suggest a method for packaging a multi-chip module, as recited in claim 1 above, that includes connecting wafer bumps in peripheral regions of first and second chips to inner leads of first and second TAB tapes, mounting the outer lead of the first TAB tape on a patterned circuit, connecting an outer lead of the second TAB tape to a wafer bump in a peripheral region of a third chip, connecting an inner lead of a third TAB tape to another wafer bump in the peripheral region of the third chip, and connecting wafer bumps in a peripheral region of a fourth chip to the outer lead of the second TAB tape and the inner lead of the third TAB tape.

Consequently, Isaacson fails to cure all of the salient deficiencies of Moon et al. with regard to the present claim 1. As a result, the present claim 1 and all claims dependent directly or indirectly therefrom (including claims 4 and 8) are fully patentable over Moon et al. and Isaacson. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 5-6 and 9-10 under 35 U.S.C. § 103

The rejection of Claim 5-6 and 9-10 under 35 U.S.C. § 103 as being unpatentable over Moon et al. in view of Morrison et al. is respectfully traversed.

Claims 5-6 and 9-10 also depend from claim 1. Therefore, claims 5-6 and 9-10 include the same limitations as claim 1 above. As explained above, Moon et al. is saliently deficient with regard to the present claim 1, and for essentially the same reasons as for claim 1, claims 5-6 and 9-10 are patentable over Moon et al. in view of Morrison et al.

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Morrison et al. discloses a vertical stack of semiconductor devices, formed by folding a strip-like flexible interconnector assembled with integrated circuit chips, packages and/or passive components and attaching coupling members solderable to other parts (Abstract). Morrison et al. further discloses a single interconnector 101 or 201, that is used to couple from 2 to 4 integrated circuit die (see, e.g., paragraphs [0051], [0067] and [0070]. pp. 3 and 5, and FIGS. 1(A)-(B), 1(D), 1(G)-(H), 2(A)-(B), and 2(D)-(I)). As a result, Morrison et al. do not cure the deficiencies of Moon et al. with regard to the present claim 1 (namely, connecting wafer bumps in peripheral regions of a plurality of chips to a plurality of inner and/or outer leads of TAB tapes).

As a result, the presently claimed invention is fully patentable over Moon et al. and Morrison et al. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all grounds for rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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